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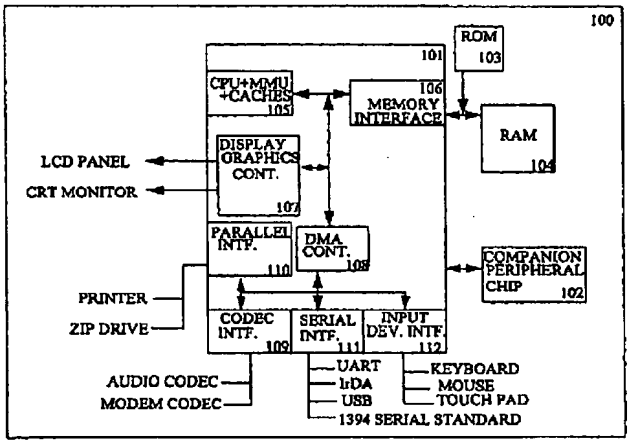

(57) Abstract

A programmable Power Management Unit (PMU) is provided. The Power Management Unit (PMU) supports a number of different power states namely a normal power state, a software-controlled sleep power state, a hardware-controlled sleep power state, and two register programmable power states. In the normal power state, all circuits in the integrated circuit (e.g., graphics/display controller) are enabled. In the software-controlled sleep power state, all circuits in the integrated circuit are disabled except for frame buffer memory refresh logic and part of the bus interface. In the hardware-controlled sleep power state, all circuits in the integrated circuit are disabled except for the memory interface logic. In the two register programmable power states, circuits can be selectively powered up or down as desired in a single power sequencing. Moreover, under the present invention, the interval between circuits that are being disabled or enabled in a power sequencing is also programmable.

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PROGRAMMABLE AND FLEXIBLE POWER MANAGEMENT UNIT

FIELD OF THE INVENTION

The invention generally relates to computer systems, and more particularly relates to managing power sequences to disable and enable circuits.

BACKGROUND OF THE INVENTION

With the advances of semiconductor and computer technology, computer systems are becoming faster and at the same time smaller in size. Desk-top and even lap-top computer systems now possess processing speeds of main-frame computers that used to fill up a small room. Even hand-held computer systems such as personal digital assistants (PDA), which are becoming more popular, are getting more powerful. As computer systems become more miniaturized and inexpensive, more demands are constantly being required of them as well. One such demand is speed or performance.

At the same time, as computer systems become more powerful and more miniaturized, power-conservation also presents a difficult challenge to overcome. Because of their small size, hand-held computer systems are powered by battery which have limited operating duration. Since more power is required for faster and more powerful processors, innovative solutions are required to conserve power and thereby extend the battery operating duration.

Within each computer system are many integrated circuits designed to perform different functions such as a memory controller, a hard disk controller, a graphics/video controller, a communications controller, and other peripheral controllers. As is well-known, each of these integrated circuits is supplied a clock signal to be used as a timing reference in synchronizing the operation of the integrated circuit. In general, power consumption increases as a result of the integrated circuit being clocked faster.

Periodically, an integrated circuit is not needed and is idle insofar as system functionality is concerned. At other times, while a sub-circuit (e.g., combination logic and data path) that performs data processing and transferring in the integrated circuit is still running, other sub-circuits in the integrated circuit are idle. Because these sub-circuits continue to receive a clock signal, their respective internal sub-circuits continue to be exercised and consume significant power, even while they remain idle. Accordingly, to conserve power, the clock signal to idle sub-circuits is disabled. The clock signal to these sub-circuits are then enabled as necessary. Powering up (enabling) and powering down (disabling) selected sub-circuits in an integrated sub-circuit may occur in a required sequence. Such power sequencing is required because some sub-circuits are dependent on other sub-circuits. For example, a sub-circuit needs to be powered up before another sub-circuit can be powered up. Power sequencing is also required when a sub-circuit needs a sequence of input signals to turn on or off as in the case of some synchronous dynamic Random Access Memory (RAM) or a Liquid Crystal Display (LCD) flat panel monitor. Such power sequence is important because if the sequence is not done properly then some circuitry blocks will not be enabled properly.

Power Management Units (PMUs) are typically used to provide the desired power sequencing. Conventional PMUs, however, can only power up or power down selected sub-circuits in one sequence. In other words, conventional PMUs do not have the capability to power up selected sub-circuits and power down other selected sub-circuits in the same sequence. This inflexibility greatly restricts the power sequencing applications of conventional PMUs. Moreover, the power sequences in conventional PMUs are normally predefined which further restrict the applications of conventional PMUs.

Thus, a need exists for a PMU that allows for power up sequencing as well as power down sequencing to occur in one sequence and for selectively powering up and powering down circuits in a power sequence.

SUMMARY OF THE INVENTION

The present invention meets the above need with a programmable and flexible Power Management Unit (PMU). The PMU comprises: a counter circuit, a state machine, a decoder, and a plurality of enable circuits. The counter circuit receives as inputs interval control signals. The counter circuit monitors power sequencing intervals in response to the interval control signals. The counter circuit generates signals indicating whether the power sequencing intervals have expired. The state machine receives as inputs the power sequencing interval status signals and state control signals. In response to the state control signals, the state machine selects a main power state for the PMU, wherein each main power state has N sub-states organized in a sequence. In response to the power sequencing interval status signals, the state machine selectes a sub state for the PMU. The state machine generates signals indicating the main power state and sub-state that the state machine is currently engaged.

The decoder circuit receives as inputs the signals from the state machine. In response to the signals from the state machine, the decoder circuit monitors status of the main power state and sub-state that the state machine is currently engaged in and generates status signals to indicate the status of the main power state and sub-state. The plurality of enable circuits receives as inputs the signals from the state machine, the status signals from the decoder circuit, and select signals. The plurality of enable circuits generates signals to enable selected circuits.

All the features and advantages of the present invention will become apparent from the following detailed description of its preferred embodiment whose description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a high-level block diagram illustrating a typical computer system that implements the present invention.

Figure 2 is a block diagram illustrating in greater detail graphics/display controller 107 illustrated in Figure 1.

Figure 3 is a block diagram illustrating in greater detail Power Management Unit 205 illustrated in Figure 2.

Figure 3A is a diagram illustrating in greater detail state machine circuit 301 of Figure 3.

Figure 4 is a first state diagram illustrating some of the relevant states performed by PM state machine 351 illustrated in Figure 3A.

Figure 5 is a second state diagram illustrating other relevant states performed by PM state machine 351 illustrated in Figure 3A.

Figure 6 is a block diagram illustrating in greater detail an embodiment of counter circuit 302 illustrated in Figure 3.

Figure 7 is a block diagram illustrating in greater detail an embodiment of decoder circuit 303 illustrated in Figure 3.

Figure 8 is a block diagram illustrating in greater detail an embodiment of clock enable circuit 304 illustrated in Figure 3.

Figure 9A is a block diagram illustrating in greater detail an embodiment of memory enable circuit 305 illustrated in Figure 3.

Figure 9B is a block diagram illustrating in greater detail an alternate embodiment of memory enable circuit 305' illustrated in Figure 3.

Figure 10 is a block diagram illustrating in greater detail an embodiment of display enable circuit 306 illustrated in Figure 3.

Figure 11 is a block diagram illustrating in greater detail an embodiment of flat panel enable circuit 307 illustrated in Figure 3.

Figures 11A-11G are exemplary timing diagrams of the power-up sequence associated with flat panel enable circuit 307.

Figures 11H-11N are exemplary timing diagrams of the power-down sequence associated with flat panel enable circuit 307.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects

of the present invention. While the following detailed description of the present invention describes its application in the area involving a graphics/display controller, it is to be appreciated that the present invention is also applicable to any application involving multiple data paths such as communications, core logic, central processing units (CPU), and others.

In accordance to a preferred embodiment of the present invention, the Power Management Unit (PMU) supports five different power states: a normal power state, a software-controlled sleep power state, a hardware-controlled sleep power state, and two register programmable power states. In the normal power state, all circuits in the integrated circuit (e.g., graphics/display controller) can be enabled. In the software-controlled sleep power state, all circuits in the integrated circuit are disabled except for frame buffer memory refresh logic (which can be optionally enabled) and part of the bus interface. In the hardware-controlled sleep power state, all circuits in the integrated circuit are disabled except for the frame buffer memory refresh logic which can be optionally enabled. In the two register programmable power states, circuits can be selectively enabled or disabled as desired. Under the present invention, additional pre-defined power states as well as programmable power states can be added beyond the five power states discussed above.

Accordingly, under the present invention, the programmable power states allow the user to completely decide which module is to be disabled and which is not to be disabled (i.e., is enabled and can be enabled). Furthermore, in accordance to the present invention, the interval between circuits that are being disabled or enabled in a power sequence is also programmable.

Reference is now made to Figure 1 illustrates, for example, a high-level diagram of computer system 100 upon

which the present invention may be implemented or practiced. More particularly, computer system 100 may be a laptop or hand-held computer system. It is to be appreciated that computer system 100 is exemplary only and that the present invention can operate within a number of different computer systems including desk-top computer systems, general purpose computer systems, embedded computer systems, and others.

As shown in Figure 1, computer system 100 is a highly integrated system which includes of integrated processor circuit 101, peripheral controller 102, read-only-memory (ROM) 103, and random access memory (RAM) 104. The highly integrated architecture allows power to be conserved. Computer system architecture 100 may also include a peripheral controller if there is a need to interface with complex and/or high pin-count peripherals that are not provided in integrated processor circuit 101.

While peripheral controller 102 is connected to integrated processor circuit 101 on one end, ROM 103 and RAM 104 are connected to integrated processor circuit 101 on the other end. Integrated processor circuit 101 comprises a processing unit 105, memory interface 106, graphics/display controller 107, direct memory access (DMA) controller 108, and core logic functions including encoder/decoder (CODEC) interface 109, parallel interface 110, serial interface 111, input device interface 112, and flat panel interface (FPI) 113. Processing unit 105 integrates a central processing unit (CPU), a memory management unit (MMU), together with instruction/data caches.

CODEC interface 109 provides the interface for an audio source and/or modem to connect to integrated processor circuit 101. Parallel interface 110 allows parallel input/output (I/O) devices such as hard disks, printers, etc. to connect to integrated processor circuit 101. Serial interface 111 provides the interface for serial I/O devices such as universal asynchronous receiver transmitter (UART)

to connect to integrated processor circuit 101. Input device interface 112 provides the interface for input devices such as keyboard, mouse, and touch pad to connect to integrated processor circuit 101.

DMA controller 108 accesses data stored in RAM 104 via memory interface 106 and provides the data to peripheral devices connected to CODEC interface 109, parallel interface 110, serial interface 111, or input device interface 112. Graphics/display controller 107 requests and accesses the video/graphics data from RAM 104 via memory interface 106. Graphics/display controller 107 then processes the data, formats the processed data, and sends the formatted data to a display device such as a liquid crystal display (LCD), a cathode ray tube (CRT), or a television (TV) monitor. In computer system 100, a single memory bus is used to connect integrated processor circuit 101 to ROM 103 and RAM 104.

In the preferred embodiment, the invention is implemented as part of graphics/display controller 107. To be more precise, the invention is implemented inside PMU 205 which is a component of graphics/display controller 107. Reference is now made to Figure 2 illustrating graphics/display controller 107 in greater detail. In general, graphics/display controller 307 comprises CPU Interface Unit (CIF) 201, frame buffer, 202, Phase Lock Loop (PLL) circuit 203, oscillator 204, Power Management Unit (PMU) 205, Graphics Engine (GE) 206, Memory Interface Unit (MIU) 207, display controller 1&2 (DC1 & DC2) 208, Flat Panel Interface (FPI) 209, CRT Digital-to-Analog Converter (DAC) 210, and master mode module 211. CIF 201 provides the interface to processing unit 105 and DMA controller 108. Accordingly, CIF 201 routes requests and data received from processing unit 105 to the desired destination. In particular, CIF 201 sends register read/write requests and memory read/write requests from the host CPU processing unit 105 and DMA controller 108 to the appropriate modules in graphics/display controller 107. For example, memory

read/write requests are passed on to MIU 207 which in turn reads/writes the data from/to frame buffer 202. CIF 201 also serves as the liaison with DMA controller 108 to fetch data from system memory (ROM 103 and RAM 104) and provides the data to GE 206 and MIU 207. Further, CIF 201 has a power mode register PMCSR that is programmable by the host CPU in processing unit 105 to control the power state of graphics/display controller 107.

Frame buffer 202 is used to store the display image as well to act as a temporary buffer for various purposes. Oscillator 204 provides a reference clock signal to PLL circuit 203 which in turn generates three programmable phase lock loop clock signals: PLL1, PLL2, and PLL3 for the different modules in graphics/display controller 107. More particularly, while clock signal PLL1 is used for GE 206 and MIU 207, clock signals PLL2 and PLL3 are used for display controller 1&2 (DC1 & DC2) 208. PMU 205 monitors PMCSR register in CIF 201 together with external signal PDWNLI to determine the desired power state. In turn, PMU 205 enables or disables the different modules as well as performs the required power-on and power-off sequence of the different modules as pertaining to a particular power state. GE 206 processes graphics image data stored in frame buffer 202 based on commands issued by the host CPU. Master mode module 211 allows GE 206 to fetch queued commands in system memory (ROM 103 and RAM 104) which are issued by the host CPU.

MIU 207 controls all read and write transactions from/to frame buffer 202.. Such read and write requests may come from the host CPU via CIF 201, GE 206, display controller 1&2 (DC1 & DC2) 208, FPI 209 etc. Display controller 208 retrieves image data from frame buffer 202 via MIU 207 and serializes the image data into pixels before outputting them to FPI 209 or CRT DAC 210. Accordingly, display controller 1&2 208 generates the required horizontal and vertical display timing signals. If the display device

involved is a LCD, pixel data from display controller 208 is sent to FPI 209 before being passed on to the LCD. In the preferred embodiment, display controller 1&2 208 comprises a display controller 1 (DC1) that is normally used for a flat panel display (FPD) and a display controller 2 (DC2) that is normally used for a CRT. FPI 209 further processes the data by further adding different color hues or gray shades for display. Additionally, depending on whether a thin film transistor (TFT) LCD (a.k.a., active matrix LCD) or a super twisted nematic (STN) LCD (a.k.a., passive matrix LCD) is used, FPI 209 formats the data to suit the type of display. Furthermore, FPI 209 allows color data to be converted into monochrome data in the event a monochrome LCD is used. Conversely, if the display device is a cathode ray tube (CRT), pixel data is provided to CRT digital-to-analog converter (DAC) 210 prior to being sent to the CRT. CRT DAC 210 converts digital pixel data from display controller 208 to analog Red Green and Blue (RGB) signals to be displayed on the CRT monitor.

Reference is now made to Figure 3 illustrating in greater detail PMU 205 which implements the present invention. As shown in Figure 3, PMU 205 includes state machine circuit 301, counter circuit 302, decoder 303, clock enable circuit 304, memory enable circuit 305, display enable circuit 306, flat panel enable circuit 307, buffers 308-309, and inverter 310. Chip reset signal CCRSTL is buffered by buffer 308 whose output signal PMRSTL is used to reset state machine to D3 state. Signal PMRSTL is provided as input to state machine circuit 301 and counter circuit 302. Power management clock signal PMCLKI is provided as input to buffer 309 and inverter 310 which in turn output signals PMCLK and PMCLKL, respectively. Accordingly, signal PMCLKL is the invert of signals PMCLKI and PMCLK. In the present embodiment, power management clock signal PMCLKI is approximately 16.384 kHz. Clock signals PMCLKL and PMCLK are provided as input to state machine circuit 301 and counter circuit 302, respectively. State machine circuit

301 is clocked on the rising edge of clock signal PMCLKL. All incoming signals of state machine circuit 301 are generated on the rising edge of clock signal PMCLK. The rising edge of signal PMCLK lags behind the rising edge of clock signal PMCLKL by 180 degrees. In so doing, sufficient set and hold time are provided for state machine circuit 301 to minimize problems associated with clock skew thereby allowing valid information carried by its incoming signals to be latched. In addition, the output signals of state machine circuit 301 and decoded output signals generated by decoder output 303 are latched at the rising edge of clock PMCLK by enable circuits 304-307.

Counter circuit 302 is used to determine the time interval between the disabling or enabling of two circuits or modules in power sequencing. Such time interval is required to ensure that a circuit/module is enabled or disabled properly. In accordance to the present invention, such time interval is programmable. Preferably, there are two main types of power sequencing intervals: general power sequencing interval (hereinafter T_i) and Flat Panel power sequencing interval (hereinafter T_j). In general, a flat panel power sequencing may be required as a part of a general power sequencing. Such flat panel power sequencing may be required because a flat panel display (FPD) normally has two or three power supplies that must be enabled in a certain order. As an example, for a FPD that requires two power supplies, a first power supply must be enabled, then the flat panel control signal and the flat panel data output signal must be enabled before the second power supply is enabled. The same counter can be used for both types of power sequencing interval because they occur at different times. Ti is controlled by bits PM00R[19:18] to have a duration of 16, 32, 64, or 128 PMCLK clock cycles. Tj is controlled by bits PM00R[21:20] to have a duration of 512, 1024, 2048, or 4096 PMCLK clock cycles. In the preferred embodiment, counter circuit 302 is further be used to determine the power sequence settling time which is the

minimum waiting period between the end of a power up/power down sequencing and the next power up/power down sequencing. The power settling time is fixed to 4 PMCLK clock cycles.

State machine circuit 301 generates signal PMCE to enable or disable counter circuit 302. When enable signal PMCE is asserted HIGH, counter circuit 302 is enabled. Otherwise, when enable signal PMCE is deasserted LOW, counter circuit 302 is disabled after being reset. Clock signal PMCLK is used to drive counter circuit 302. The value of bits PM00R[19:18] is used to determine whether T_i is to have a duration of 16, 32, 64, or 128 PMCLK clock cycles. The value of bits PM00R[21:20] is used to determine whether T_j is to have a duration of 512, 1024, 2048, or 4096 PMCLK clock cycles. Accordingly, counter circuit 302 asserts signals PMCI and PMCJ, which are provided as inputs to state machine circuit 301, to indicate to state machine circuit 301 that intervals T_i and T_j have expired, respectively. Counter circuit 302 may further assert signal PMC2, which is also provided as input to state machine circuit 301, to indicate to state machine circuit 301 that counter circuit 302 has been enabled for 3 PMCLK clock cycles.

In general, state machine circuit 301 is used to determine and monitor the power states for PMU 205. Power state bits PMCSR[1:0] and signal PDWNLI, which are provided as inputs to state machine circuit 301, dictate the power state that PMU 205 is to be in. Bits PMCSR[1:0] and signal PDWNLI are decoded in state machine circuit 301 to generate power state signal PMD[4:0] which are actual inputs to state machine circuit 301. When the value of PMD[4:0] changes, it indicates that there is a change in power states and as a result, the power sequencing PM state machine will be triggered to execute a power sequencing to transition from an old power state to a new power state.

Reference is now made to Figure 3A illustrating in greater detail state machine circuit 301. As shown in

Figure 3A, state machine circuit 301 comprises PM state machine 351, AND-gates 352-355, and inverter 356. State machine circuit 301 receives input signals FPPS, MIUPS, PMCI, PMCJ, PMC2, PMCSR[1:0], PDWNLI, PMRSTL, and PMCLKL while provides output signals PMD[4:0], PMS[5:0], PMSQDONE, and PMSQACT. AND-gates 352-355 and inverter 356 combine to decode bits PMCSR[1:0] and signal to generate power state signal PMD[4:0]. More particularly, the invert of bit PMCSR[0], the invert of bit PMCSR[1], and bit PDWNLI are provided as input to AND-gate 352 which outputs bit PMD[0]. Bit PMCSR[0], the invert of bit PMCSR[1], and bit PDWNLI are provided as input to AND-gate 353 which outputs bit PMD[1]. The invert of bit PMCSR[0], bit PMCSR[1], and bit PDWNLI are provided as input to AND-gate 354 which outputs bit PMD[2]. Bit PMCSR[0], bit PMCSR[1], and bit PDWNLI are provided as input to AND-gate 355 which outputs bit PMD[3]. Bit PDWNLI is provided to inverter 356 which outputs bit PMD[4]. PM state machine 351 receives as inputs signal PMRSTL, PMCLKL, FPPS, MIUPS, PMCJ, PMCI, PMC2, and power state signal PMD[4:0]. As discussed in greater detail below, PM state machine 351 generates as output signals PMCE, PMSQDONE, PMSQACT, and PMS[5:0].

Table 1 below provides the different power states generated by decoding power state bits PMCSR[1:0] and signal PDWNLI.

PDWNLI	PMCSR[1:0]	PMD[4:0]	Power State Name
1	00	00001	D0
1	01	00010	D1
1	10	00100	D2
1	11	01000	D3
0	XX	10000	D4

Table 1

As shown in Table 1, there are five possible power states D0-D4 supported by PMU 205 in accordance to the

present invention. Under the preferred embodiment, D0 (i.e., PMD[4:0] is 00001) is a normal power state, D1 is a first register controlled programmable power state (i.e., PMD[4:0] is 00010), D2 is a second register controlled programmable power state (i.e., PMD[4:0] is 00100), D3 is a software-controlled sleep power state (i.e., PMD[4:0] is 01000), and D4 is a hardware-controlled sleep power state (i.e., PMD[4:0] is 10000). As suggested by its name, during the normal power state D0, display/graphics controller 107 is its normal functioning mode which generally means that all of its circuits and modules can be enabled (powered up). Power state D1 is a programmable power saving mode in which CIF 201 and PMU 205 are to be enabled while other circuits and modules in display/graphics controller 107 can be enabled or disabled as controlled by PM01R register. Because PM01R register is programmable by the user, the power sequencing associated with this power state is flexible in accordance to the present invention. Power state D2 is a second programmable power saving mode in which CIF 201 and PMU 205 are to be enabled while other circuits and modules in display/graphics controller 107 can be enabled or disabled as controlled by PM02R register. Because PM02R register is programmable by the user, the power sequencing associated with this power state is flexible in accordance to the present invention.

Power state D3 is a software controlled sleep mode in which power conservation is the objective. Accordingly, most circuits and modules in display/graphics controller 107 are disabled (powered down) including most sub-circuits in CIF 201. The only circuits and modules that remain enabled during power state D3 are the configuration registers in CIF 201, which contain PMCSR[1:0], and PMU 205. In addition, the memory refresh circuitry which is part of MIU 207 can be optionally enabled in D3 state as controlled by a programmable register bit. Preferably, power state D3 is the default state when display/graphics controller 107 is reset. Power state D4 is a hardware controlled sleep mode

and the lowest power saving mode. To conserve power, practically all circuits and modules in display/graphics controller 107 are disabled (powered down) including all sub-circuits in CIF 201. The only module that remains enabled during power state D4 is PMU 205. Additionaly, the memory refresh circuitry which is part of MIU 207 can be optionally enabled in D4 state as controlled by a programmable register bit.

As shown in Table 1, input signal PWDNLI is used to control the hardware controlled sleep mode D4. When signal PWDNLI is HIGH, it is combined with different permutations of bits PMCSR[1:0] to form four different power states (D0-D3). When signal PWDNLI is LOW, it can be combined with any permutations of bits PMCSR[1:0] to form the remaining power state (D4).

PM state machine circuit 351 further receives as inputs signals MIUPS, FPPS, and PMRSTL. Signals MIUPS and FPPS are used to trigger power sequencing when MIU 207 or FPI 209 is enabled/disabled, respectively. PM state machine 351 also receives signal PMCI, PMCJ, and PMC2 which are outputs of counter circuit 302. Signal PMRSTL, which is active LOW, is used to reset PM state machine 351. In addition to outputting signal PMCE and power states signals PMD[4:0] as discussed earlier, PM state machine 351 further outputs signals PMS[5:0], PMSQDONE, and PMSQACT. While signal PMSQACT indicates that the current general power sequencing is occurring, signal PMSQDONE indicates that the current general power sequencing is complete. State encoding signal PMS[5:0] is used to indicate all the states in PM state machine 351. Table 2 provides the machine states of PM state machine 351.

State Name	State Encoding PMS[5:0]
S00	**000000**
S01	000001
S02	000010
S03	000011
S04	000100
S05	000101
S06	000110
S07	000111
S10	**001000**
S11	001001
S12	001010
S13	001011
S14	001100
S15	001101
S16	001110
S17	001111
S20	**010000**
S21	010001
S22	010010
S23	010011
S24	010100
S25	010101
S26	010110
S27	010111
S30	**011000**
S31	011001
S32	011010
S33	011011
S34	011100
S35	011101
S36	011110
S37	011111
S40	**1xx000**
S41	1xx001
S42	1xx010
S43	1xx011
S44	1xx100
S45	1xx101
S46	1xx110
S47	1xx111

Table 2

As shown in Table 2, there are five main states S00 (D0), S10 (D1), S20 (D2), S30 (D3), and S40 (D4). They are highlighted for emphasis. In the preferred embodiment, the five main states are represented (encoded) by the three most

significant PMS bits (i.e., PMS[5:3]). In the current embodiment, for each of these main states, there are seven associated sub-states Sx1-Sx7 where x = 0-to-4. However, it should be clear to a person of ordinary skill in the art that other sub-states may also be associated with each of the main power state. All the sub-states Sx1-Sx7 are represented (encoded) by the three least significant PMS bits (i.e., PMS[2:0]). The corresponding state encoding values for the main and sub states in the current embodiment, which are carried by state encoding signal PMS[5:0], are also provided in Table 2.

State encoding signal PMS[5:0] and enable signal PMCE are provided as inputs to decoder 303 which decodes these signals to generate status signals PMP[7:1], PMD0X, PMD1X, and PMD2X. Status signals PMP[7:1] are one-clock pulse signals indicating the beginning of the corresponding sub-states Sx1-Sx7 where x = 0-to-4. Status signal PMD0X is asserted when PM state machine 351 is in states S00, S01, S02, S03, S04, S05, S06, and S07. Status signal PMD1X is asserted when PM state machine 351 is in states S10, S11, S12, S13, S14, S15, S16, and S17. Status signal PMD2X is asserted when PM state machine 351 is in states S20, S21, S22, S23, S24, S25, S26, and S27. Status signals PMP[7:1] are provided as inputs to clock enable circuit 304, memory enable circuit 305, display enable circuit 306, and flat panel enable circuit 307. Status signals PMD0X, PMD1X, and PMD2X are provided as inputs to display enable circuit 306.

In accordance to the present invention, miscellaneous control register PM00R, D1 control register PM01R, and D2 control register PM02R are used to control whether a particular circuit or module is to be enabled or disabled during a power sequencing. In general, the bits in these control registers are assigned to specific circuits/modules that are to be enabled or disabled. For example, bits 0-3 of miscellaneous control register PM00R may be used to enable (power up) or disable (power down) the clock

oscillator (OSCCLK), PLL1, PLL2, and PLL3, respectively. Since the control registers are programmable by the user, it allows selected circuits/modules to be enabled or disabled as desired in a power sequence.

In general, clock enable circuit 304 generates enable signals for the oscillator, PLL1, PLL2, and PLL3. Clock enable circuit 304 receives as inputs signals PMCLK, PMRSTL, PM00R[17:16, 3:0], PM01R[3:0], and PM02R[3:0]. In addition, clock enable circuit 304 also receives as inputs signals PMD[4:0], PMP[7], and PMP[1]. In the preferred embodiment, bits 0-3 of miscellaneous control register PM00R (i.e., PM00R[0:3]) are used to enable (power up) or disable (power down) the clock oscillator (OSCCLK), PLL1, PLL2, and PLL3, respectively. Bits 16-17 of register PM00R (i.e., PM00R[17:16] are used to enable/disable memory refresh of the frame buffer 202 during state D3 and state D4, respectively. Bits 0-3 of D1 state control register PM01R are used to enable/disable the clock oscillator (OSCCLK), PLL1, PLL2, and PLL3, respectively, in D1 power state. Bits 0-3 of D2 state control register PM02R are used to enable/disable the clock oscillator (OSCCLK), PLL1, PLL2, and PLL3, respectively, in D2 power state.

Using power state signal PMD[4:0] representing the desired PMU power state (e.g., main state) as well as status bits PMP[7,1] representing the beginning of sub-states Sx7 and Sx1 where x = 0-to-4, clock enable circuit 304 determines whether to asserts enable signals PMOSCEN, PMPLL1EN, PMPLL2EN, and PMPLL3EN. Moreover, if these enable signals are to be asserted, clock enable circuit 304 determines the proper sequence that these enable signals are to be asserted. Signal PMRSTL is used to reset clock enable circuit 304. Clock signals PMCLK are used to synchronize and latch propagating signals in clock enable circuit 304.

Memory enable circuit 305 generates enable signals for the MIU, internal memory refresh, and internal memory

restricted refresh. Memory enable circuit 305 receives as inputs signals PMCLK, PMRSTL, PM01R[4], PM02R[4], and MIUENA signal. In addition, memory enable circuit 305 also receives as inputs signals PMD[2:0], PMP[6], and PMP[2]. In the preferred embodiment, MIUENA is a register bit. When bit MIUENA is HIGH, it indicates that MIU 207 is enabled (if MIU 207 can be enabled in the present power state). When bit MIUENA is LOW, it indicates that MIU 207 is disabled. Bit 4 of D1 state control register PM01R is used to enable/disable MIU 207 in D1 power state. Bit 4 of D2 state control register PM02R is used to enable/disable MIU 207 in D2 power state.

Using power state signal PMD[2:0] representing the desired power state (e.g., main state) as well as status bits PMP[6,2] representing the status of sub-states Sx6 and Sx2 where x = 0-to-4, and MIUENA signal, memory enable circuit 305 determines whether to asserts enable signal PMMIUEN. Memory enable circuit 305 further generates signal MIUPS. Signal MIUPS is asserted HIGH when MIU 207 is enabled/disabled to indicate that MIU power sequencing is needed. More particularly, if MIU 207 is enabled, a power up sequencing is needed. If MIU 207 is disabled, a power down sequencing is needed. Signal PMRSTL is used to reset memory enable circuit 305. Clock signal PMCLK is used to synchronize and latch propagating signals in memory enable circuit 305.

Display enable circuit 306 generates enable signals for GE 206, display controller 208, and CRT DAC 210. Display enable circuit 306 receives as inputs signals PMCLK, PMRSTL, PM00R[8], PM01R[27,25,24,19,17,16,8,6], and PM02R[27,25,24,19,17,16,8,6]. In addition, display enable circuit 306 also receives as inputs signals PMD[2:0], PMP[3,5], PMD0X, PMD1X, and PMD2X. In the preferred embodiment, bit 8 of miscellaneous control register PM00R (i.e., PM00R[8]) is used to enable/disable GE 206 if GE 206 can be enabled in the present power state. Bits 6, 8, 16,

17, 19, 24, 25, and 27 of D1 state control register PM01R are used to enable/disable GE 206, CRT DAC 210, display controller 1, window 1 sub-module, cursor 1 sub-module, display controller 2, window 2 sub-module, and cursor 2 sub-module in D1 power state. Similarly, bits 6, 8, 16, 17, 19, 24, 25, and 27 of D2 state control register PM02R are used to enable/disable GE 206, CRT DAC 210, display controller 1, window 1 sub-module, cursor 1 sub-module, display controller 2, window 2 sub-module, and cursor 2 sub-module in D2 power state. Bits PMD0X, PMD1X, and PMD2X, when asserted, indicate whether state machine circuit 301 is in a main state or is transitioning to the D0, D1, and D2 main state, respectively.

Using power state signal PMD[2:0] representing the desired PMU power state (e.g., main state), status bits PMP[3,5] representing the beginning of sub-states Sx3 and Sx5 where x = 0-to-4, signal DCDACENA, signal DC1ENA, and signal DC2ENA, display enable circuit 306 determines whether to asserts enable signals PMGEEN, PMDACEN, PMDC1EN, and PMDC2EN. Moreover, using status signals PMD0X, PMD1X, PMD2X, display enable circuit 306 determines whether to asserts enable signals PMDC1WEN, PMDC1CEN, PMDC2WEN, and PMDC2CEN. More particularly, enable signals for the display controller 1 of display controller 208 include: PMDC1EN, PMDC1WEN, and PMDC1CEN. Enable signals for the display controller 2 of display controller 208 include: PMDC2EN, PMDC2WEN, and PMDC2CEN. If the enable signals above are to be asserted or deasserted, display enable circuit 306 determines the proper sequence that these enable signals are to be asserted. Signal DCDACENA is used to enable CRT DAC 210 when CRT DAC 210 can be enabled in the current power state. Signals DC1ENA and DC2ENA indicate whether the display controller 1 and the display controller 2 are to be enabled, respectively. Signal PMRSTL is used to reset display enable circuit 306. Clock signal PMCLK is used to synchronize and latch propagating signals in display enable circuit 306.

Flat Panel enable circuit 307 generates enable signals for FPI 209, flat panel power sequencing, and PWM enable. Flat panel enable circuit 307 receives as inputs signals PMCLK, PMRSTL, PM01R[9], PM02R[9], FPIENA, and DCFPIENA. In addition, flat panel enable circuit 307 also receives as inputs signals PMD[2:0] and PMP[5:3]. In the preferred embodiment, bit 9 of D1 control register PM01R (i.e., PM01R[9]) is used to enable/disable the flat panel display in the D1 power state. Similarly, bit 9 of D2 control register PM02R (i.e., PM02R[9]) is used to enable/disable the flat panel display in the D2 power state. FPIENA and DCFPIENA are control bits. When bit FPIENA is HIGH, it indicates that FPI 209 is enabled if FPI 209 can be enabled in the current power state. When bit DCFPIENA is HIGH, it indicates that either DC1 or DC2 of display controller 1&2 208, which is selected to drive FPI 209, is enabled.

Using power state signal PMD[2:0] representing the desired power state (e.g., main state), signal FPIENA, signal DCFPIENA, as well as status bits PMP[5:3] representing the beginning of sub-states Sx3, Sx4, and Sx5 where x = 0-to-4, flat panel enable circuit 307 determines whether to asserts enable signals PMENVDD, PMENCTL, and PMENVEE. The enable signal for FPI 209 is PMENCTL. The enable signals for flat panel power sequencing include PMENVDD, PMENCTL, and PMENVEE. If these enable signals are to be asserted, flat panel enable circuit 307 determines the proper sequence that these enable signals are to be asserted. Flat panel enable circuit 307 further generates signal FPPS which is asserted HIGH when the flat panel display is enabled or disabled to indicate that flat panel power sequencing is needed. Signal PMRSTL is used to reset flat panel enable circuit 307. Clock signal PMCLK is used to synchronize and latch propagating signals in flat panel enable circuit 307.

Figure 4 is a state diagram which illustrates some of the relevant states in PM state machine 351 that was illustrated in Table 2. In the preferred embodiment, no matter what PM state machine 351 may be in at the time, state S30 (D3) becomes the default state whenever reset signal PMRSTL is asserted LOW. From state S30, PM state machine 351 monitors power state signal PMD[4:0] to determine whether the power state has changed. If signal PMD[4:0] has the binary value 01000 indicating that the desired power state is D3, PM state machine 351 remains in state S30. If signal PMD[4:0] changes to binary value of 10000 indicating that the desired power state is D4, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S41. If signal PMD[4:0] changes to binary value of 00001 indicating that the desired power state is D0, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S01. If signal PMD[4:0] changes to binary value of 00010 indicating that the desired power state is D1, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S11. Finally, if signal PMD[4:0] changes to binary value of 00100 indicating that the desired power state is D2, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S21.

If PM state machine 351 is currently engaged in state S40 (D4), PM state machine 351 monitors power state signal PMD[4:0] to determine whether the power state has changed. If signal PMD[4:0] has the binary value 10000 indicating that the desired power state is D4, PM state machine 351 remains in state S40. If signal PMD[4:0] changes to binary value of 00001 indicating that the desired power state is D0, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S01. If signal PMD[4:0] changes to binary value of 00010 indicating that the desired power state is D1, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and

switches to state S11. If signal PMD[4:0] changes to binary value of 00100 indicating that the desired power state is D2, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S21. Finally, if signal PMD[4:0] changes to binary value of 01000 indicating that the desired power state is D3, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S31.

If PM state machine 351 is currently engaged in state S00 (D0), PM state machine 351 monitors power state signal PMD[4:0] to determine whether the power state has changed as well as monitors signal MIUPS and FPPS to determine whether MIU or flat panel power sequencing needs to be initiated. If signal PMD[4:0] has the binary value of 00001 indicating that the desired power state is D0, PM state machine 351 next monitors signals MIUPS and FPPS to determine whether MIU or FPI is being enabled/disabled therefore requiring power sequencing. In the event either a MIU power sequencing or a flat panel power sequencing is required, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S01. Otherwise, if signal PMD[4:0] has the binary value 00001 indicating that the desired power state is D0 and signals MIUPS and FPPS are deasserted indicating that neither MIU nor flat panel sequencing is needed, PM state machine 351 remains in state S00.

If signal PMD[4:0] changes to binary value of 10000 indicating that the desired power state is D4, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S41. If signal PMD[4:0] changes to binary value of 01000 indicating that the desired power state is D3, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S31. If signal PMD[4:0] changes to binary value of 00100 indicating that the desired power state is D2, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and

switches to state S21. Finally, if signal PMD[4:0] changes to binary value of 00010 indicating that the desired power state is D1, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S11.

If PM state machine 351 is currently engaged in state S10 (D1), PM state machine 351 monitors power state signal PMD[4:0] to determine whether the power state has changed as well as monitors signal MIUPS and FPPS to determine whether MIU or flat panel power sequencing needs to be initiated. If signal PMD[4:0] has the binary value of 00010 indicating that the desired power state is D1, PM state machine 351 next monitors signals MIUPS and FPPS to determine whether a MIU power sequencing or a flat panel power sequencing is needed. In the event either a MIU power sequencing or a flat panel power sequencing is required, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S11. Otherwise, if signal PMD[4:0] has the binary value 00010 indicating that the desired power state is D1 and signals MIUPS and FPPS are deasserted indicating that neither MIU nor flat panel sequencing is needed, PM state machine 351 remains in state S10.

If signal PMD[4:0] changes to binary value of 00001 indicating that the desired power state is D0, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S01. If signal PMD[4:0] changes to binary value of 10000 indicating that the desired power state is D4, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S41. If signal PMD[4:0] changes to binary value of 01000 indicating that the desired power state is D3, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S31. Finally, if signal PMD[4:0] changes to binary value of 00100 indicating that the desired power state is D2, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S21.

If PM state machine 351 is currently engaged in state S20 (D2), PM state machine 351 monitors power state signal PMD[4:0] to determine whether the power state has changed as well as monitors signal MIUPS and FPPS to determine whether MIU or flat panel power sequencing needs to be initiated. If signal PMD[4:0] has the binary value of 00100 indicating that the desired power state is D2, PM state machine 351 next monitors signals MIUPS and FPPS to determine whether a MIU power sequencing or a flat panel power sequencing is needed. In the event either a MIU power sequencing or a flat panel power sequencing is required, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S21. Otherwise, if signal PMD[4:0] has the binary value 00100 indicating that the desired power state is D2 and signals MIUPS and FPPS are deasserted indicating that neither MIU nor flat panel sequencing is needed, PM state machine 351 remains in state S20.

If signal PMD[4:0] changes to binary value of 01000 indicating that the desired power state is D3, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S31. If signal PMD[4:0] changes to binary value of 10000 indicating that the desired power state is D4, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S41. If signal PMD[4:0] changes to binary value of 00001 indicating that the desired power state is D0, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S01. Finally, if signal PMD[4:0] changes to binary value of 00010 indicating that the desired power state is D1, PM state machine 351 deasserts signal PMCE to disable counter circuit 302 and switches to state S11.

Reference is now made to Figure 5 illustrating a continuation state diagram of the states in PM state machine 351. More specifically, Figure 5 picks up where Figure 4 leaves off when sub-states S01, S11, S21, S31, and S41 are reached. It is to be appreciated that all the states in

Figures 4-5 are carried out by PM state machine 351. However, for the sake of clarity, these states are separated into two separate Figures 4 and 5. In Figure 5, the variable x can be any value between 0-4. For example, depending on the value of x, Sx1 may be sub-state S01, S11, S21, S31, and S41. As shown in Figure 5, the sub-states in Figure 5 make up a sequential sequence (Sx1-Sx7) before going back to the main state (Sx0). In short, the sub-states illustrated in Figure 5 represent a general power sequencing when transitioning to a corresponding main power state (e.g., S00 (D0), S10 (D1), S20 (D2), S30 (D3), and S40 (D4)).

As such, when sub-state Sx1 is arrived at from a main state according to the state diagram in Figure 4, PM state machine 351 monitors signal PMCI which indicates whether the general power sequencing interval T_i has expired. PM state machine 351 remains in sub-state Sx1 until the power sequencing interval T_i expires. As discussed earlier, general power sequencing interval T_i provides the necessary time for circuits/modules, that are not related to flat panel power sequencing, to be disabled or enabled properly. If signal PMCI is deasserted indicating that power sequencing interval T_i is still going on, PM state machine 351 ensures that signal PMCE is set HIGH to enable counter circuit 302 and remains in sub-state Sx1. Otherwise, if signal PMCI is asserted indicating that power sequencing interval T_i has expired, PM state machine 351 sets signal PMCE LOW to disable and reset counter circuit 302 and switches to the next sub-state Sx2 in the power sequencing. Like in the previous sub-state Sx1, PM state machine 351 remains in sub-state Sx2 until the power sequencing interval T_i expires. When the power sequencing interval T_i expires as indicated by signal PMCI being asserted HIGH, PM state machine 351 sets signal PMCE LOW to disable and reset counter circuit 302 and switches to the next sub-state Sx3 in the general power sequencing.

During a general power sequencing, a flat panel power sequencing may be required. As such, for sub-state Sx3, PM state machine 351 monitors signal FPPS and PMCJ in additional to signals PMCI. As discussed earlier, when asserted HIGH, signal FPPS indicates that a flat panel power sequencing is required. When asserted HIGH, signal PMCJ indicates that flat panel power sequencing interval T_j has expired. PM state machine 351 remains in state Sx3 if signal FPPS is HIGH but signal PMCJ is LOW. Likewise, PM